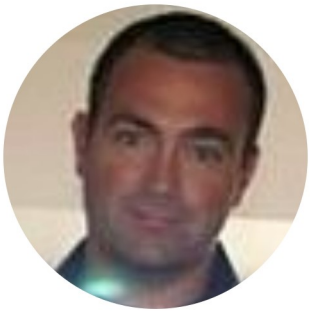
Exhibit 34



Jason [JT] Scott · 3rd

Senior Member of Technical Staff - Volume Scan Diagnostics Program Principal - Yield Engineering - CPU/GPU/Game Console

- AMD
- Nova Scotia Institute of Technology

Austin, Texas, United States · **Contact info**

500+ connections

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About

Stong technical leadership and program ownership skills. 19+ years in the semiconductor industry. Results oriented with strong leadership abilities. Experienced in the global economy, with time spent overseas. Product development expert with successful project management track record. Competitive analysis and IP intelligence.

Specialties: Volume Scan Diagnostics analysis for advanced process technology systrmatic defect identification, electrical fault isolation, memory product development, root cause microprocesspor / memory silicon debug, Lean Six Sigma based project management, engineering management, high speed signal analysis, memory bit cell engineering, failure analysis, device characterization, device qualification, yield enhancement, physical design, verification, reverse engineering, reliability test, patent intelligence, verilog

Activity

584 followers

Jason [JT] hasn't posted lately

Jason [JT] hasn't posted lately

Jason [JT]'s recent posts and comments will be displayed here.

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Experience

Member of Technical Staff - Fault Isolation Product Manager; Server/Console

AMD
Aug 2010 - Present · 12 yrs 8 mos
Austin, TX

• Electrical Fault Isolation - Device Analysis Department
• Responsible for electrical fault isolation on AMD's advanced 32nm, 28nm, 20nm APU / CPU architectures throughout; NPI, Qualification, Yield enhancement and Customer Return cycles
• Product owner for Game Console (Xbox / Playstation) and Server products
• FEOL / BEOL defect isolation
• Backside laser / emission based tool; silicon debug, characterization and defect based root cause determination
• Synopsys Camelot CAD database translation and management

Product Line Manager

Sidense
Feb 2009 - Aug 2010 · 1 yr 7 mos
Ottawa, Canada Area

• Responsible for OTP NVM silicon debug and device characterization across 6 foundries in process nodes from 28nm-180nm... ...see more

Staff Engineer - Product Engineering; Design Analysis

Qimonda
Mar 2004 - Jan 2009 · 4 yrs 11 mos
Cary, NC

• Team Lead for complete design verification and analysis coordination within the product engineering team for various Graphics, Low P ...see more

Staff Engineer - Design Center Enablement

Qimonda Technologies (Suzhou) Co., Ltd.
Jun 2008 - Nov 2008 · 6 mos
Suzhou, Jiangsu, China

• 1Gb 65nm DDR2 design verification and low voltage root cause failure identification... ...see more

Manager R&D (functional), Memory Bit Cell Design
MoSys
Sep 2002 - Apr 2003 · 8 mos
Ottawa, Canada Area

• Manage and coordinate team of Test Engineers from project specification through device evaluation... ...see more

Show all 9 experiences →

Education

Nova Scotia Institute of Technology
Electronics Engineering, Electronincs
1995 - 1997

Skills

Fault Isolation

Endorsed by 2 colleagues at AMD

2 endorsements

Failure Analysis

Endorsed by Danielle Dunn and 2 others who are highly skilled at this

Endorsed by 5 colleagues at AMD

12 endorsements

Laser Voltage Probe

Show all 33 skills →

Recommendations

Received Given

Shane Sanders · 3rd
MTS at AMD
December 24, 2008, Shane worked with Jason [JT] on the same team

Jason and I have worked together in the Design Analysis group at Qimonda for nearly 5 years. During that time he has proven to be a strong technical contributor as well as a very effective team leader for the development of low power, commodity, and graphics DRAM products. As a technical...

Eric Cordes · 3rd
Vice President GaN Technology Program at Infineon Technologies
December 21, 2008, Eric was senior to Jason [JT] but didn't manage Jason [JT] directly

I know Jason Scott since early in 2004 when he applied for the Qimonda Development Center RTP in Cary, NC, USA (at that time still Infineon). From then on Jason has demonstrated his excellence in many areas: design verification and analysis, utilization of a multitude of test equipment,...

Jens Niemax · 3rd
Scientist at Technical University of Munich
December 20, 2008, Jens managed Jason [JT] directly

I worked together with Jason during his time at the Qimonda development center in China. In theory, I was his direct manager. In reality however, we were on equal terms; both doing our part to make the development center a success. ...

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Interests

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TSMC
423,381 followers
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MTS at AMD
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Abdullah Yassine • 3rd
Principal Member of Technical Staff at Advanced Micro Devices
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Ramakanth Kondagunturi • 3rd
Principal SoC Architect at AMD
Message

Arun Sivasubramanian • 3rd
Member Of Technical Staff at AMD
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Geoff Bacon • 3rd+
R&D S&E Mechanical Engineer at Department of Energy
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Business Development Manager
Connect

Katelyn Kasella
Marketing and Communications Coordinator at Robins Kaplan LLP
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Marc Betinsky
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Katie Bennett
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Ricardo Ehramjian
Senior A/V Engineer, Trial Consultant and Multimedia Expert at Robins Kaplan LLP

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